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Notice of Allowability	Application No.	Applicant(s)	
	09/197,993	LOVETTE, STEVEN EUGENE	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
 All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 05/10/2007.
2. ☒ The allowed claim(s) is/are 26-31, 33-35, 38-43 and 45-47, now renumbered as 1-18.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying Indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____. |

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Applicants' attorneys, Mr. John Mockler and Brooks Taylor, on 07/20/2007.

Please amend claims 26, 32-38, 44-49 as follows:

26. (Currently Amended) A method for detecting corruption associated with a stack in a storage device, the stack encompassing a range of memory of a fixed size, the method comprising the steps of:

storing a first predetermined value in a first address location immediately preceding the range of memory;

storing a second predetermined value in a second address location immediately following the range of memory;

detecting the occurrence of a stack operation within the stack;

comparing a value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location, and

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where the stack operation is determined to have corrupted the first predetermined value, restoring the first predetermined value to the first address location;

comparing a value in the second address location to the second predetermined value to determine if the stack operation corrupted the second predetermined value stored in the second address location; and

where the stack operation is determined to have corrupted the second predetermined value, restoring the second predetermined value to the second address location.

32. (Canceled).

33. (Currently Amended) The method as set forth in Claim ~~32~~ 26, wherein the second predetermined value comprises a known bit pattern.

34. (Currently Amended) The method as set forth in Claim ~~32~~ 26, wherein the second predetermined value comprises a processor readable address.

35. (Currently Amended) The method as set forth in Claim ~~32~~ 26, wherein the second predetermined value comprises a processor readable instruction.

36. (Cancelled).

37. (Cancelled).

38. (Currently Amended) A system for detecting corruption associated with a stack, the system comprising:

a processor; and

a storage medium comprising a stack, the stack encompassing a range of memory of a fixed size, wherein the processor is operable to:

store a first predetermined value in a first address location immediately preceding the range of memory;

storing a second predetermined value in a second address location immediately following the range of memory;

detect the occurrence of a stack operation within the stack;

compare a value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location;

and

where the stack operation is determined to have corrupted the first predetermined value, restoring the first predetermined value to the first address location;

comparing a value in the second address location to the second predetermined value to determine if the stack operation corrupted the second predetermined value stored in the second address location; and

where the stack operation is determined to have corrupted the second predetermined value, restoring the second predetermined value to the second address location.

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44. (Canceled).

45. (Currently Amended) The system as set forth in Claim-44-38, wherein the second predetermined value comprises a known bit pattern.

46. (Currently Amended) The system as set forth in Claim-44-38, wherein the second predetermined value comprises a processor readable address.

47. (Currently Amended) The system as set forth in Claim-44-38, wherein the second predetermined value comprises a processor readable instruction.

48. (Canceled).

49. (Canceled).

2. The following is an examiner's statement of reasons for allowance:

With respect to claims 26-31, 33-35, 38-43, 45-47, the prior art of record, individually or in combination, fails to teach, suggest or render obvious the claimed invention in combination with the specific added limitations as recited in claims 26 and 38. Specifically, inter alias, the prior art of record fails to teach or suggest a method and system for store a first predetermined value in a first address location immediately preceding the range of memory; storing a second predetermined value in a second address location immediately following the range of memory;

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detect the occurrence of a stack operation within the stack; compare a value in the first address location to the first predetermined value to determine if the stack operation corrupted the first predetermined value stored in the first address location; where the stack operation is determined to have corrupted the first predetermined value, restoring the first predetermined value to the first address location; comparing a value in the second address location to the second predetermined value to determine if the stack operation corrupted the second predetermined value stored in the second address location; and where the stack operation is determined to have corrupted the second predetermined value, restoring the second predetermined value to the second address location (as disclosed in specification pages 11-15; and Figure 4).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex schedule.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Flynn Nathan can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dustin Nguyen
Examiner
Art Unit 2154

